IN THE CLAIMS:

Please cancel claims 14-17, 21, 22, 24, 38-41, 45, 46, and 48. Replace pending claims 7, 12, 13, 31, and 37, with the following clean versions of these claims.

B2

7. The method of claim 1 wherein the step of compiling comprises the steps of:

mapping predetermined C-type programming language expressions to functionally equivalent HDL program language expressions; and

assigning input/output as defined in the C-type program to specific wires in the HDL synthesizable design; and further comprising the step of:

configuring in the HDL synthesizable design an interface for a gate-level hardware representation.

B3

12. The method of claim 7, wherein the step of compiling further comprises the step of compiling C-type programming language structure assignment, structure function parameters, and structure function return values into HDL synthesizable expressions.

13. The method of claim 1 wherein the step of compiling comprises the steps of:

compiling a C-type program control flow into an HDL state machine; and

assigning input/output as defined in the C-type program to specific wires in the HDL synthesizable design; and further comprising the step of:

configuring in the HDL synthesizable design an interface for a gate-level hardware representation.

B4

31. The method of claim 25 wherein the step of compiling

comprises the steps of:

mapping predetermined C-type programming language expressions to functionally equivalent HDL program language expressions; and

assigning input/output as defined in the C-type program to specific wires in the HDL synthesizable design; and further comprising the step of:

configuring in the HDL synthesizable design an interface for a gate-level hardware representation.

37. The method of claim 25 wherein the step of compiling comprises the steps of:

compiling a C-type program control flow into an HDL state machine; and

assigning input/output as defined in the C-type program to specific wires in the HDL synthesizable design; and further comprising the step of:

configuring in the HDL synthesizable design an interface for a gate-level hardware representation.